REMARKS

Claims 1-14 and 16-30 are pending for examination with claims 1, 8, 16, 22, 27 and 28 being independent claims. No claims have been amended and no new matter has been added.

Rejections Under 35 U.S.C. §102

Claims 1-14 and 16-30 stand rejected under 35 U.S.C. §102(e) as being anticipated by Dent (U.S. Patent No. 6,680,928). Further, Claims 27-30 stand rejected under 35 U.S.C. §102(e) as being anticipated Özlütürk (U.S. Patent No. 6,366,607). Applicant respectfully disagrees and traverses as follows.

The Dent Reference

Dent is directed to a system and method for summing radio transmission signals using a set of weighting factors where the weighting factors for one signal are preferably orthogonal to weighting factors of another signal across frequency channels. (Abstract).

Claim 1 is representative of the independent claims. Claim 1 recites:

1. A method for processing signal values in a digital signal processor, the method comprising:

in response to a single instruction that specifies a plurality of signal values and a plurality of code segments of a despreading code:

complex multiplication of each signal value by a respective one of the code segments to provide a plurality of intermediate results;

complex addition of the intermediate results to provide a despread result; and

storing the despread result, wherein the complex multiplication, the complex addition and the storing of the despread result are executed in a single clock cycle of the digital signal processor.

The method of claim 1 requires that a number of actions be executed in response to a single instruction. In addition claim 1 requires that the complex addition and storing of the despread result be executed in a single clock cycle of the digital signal processor. Dent does not

disclose or suggest executing the actions of claim 1 in response to a single instruction, nor does Dent disclose or suggest executing the complex multiplication, complex addition and the storing of the despread result within a single clock cycle of the digital signal processor.

Indeed, nowhere in Dent is the operation of a digital signal processor discussed in terms of instructions or clock cycles. Dent is silent on teaching the number of instruction or clock cycles necessary to perform the operations discussed therein. On Page 3 of the Office Action the Examiner cites Dent as teaching the elements of claim 1 but nowhere does the Examiner cite Dent as teaching, disclosing or suggesting that the operation of claim 1 happen "in response to a single instruction," or that the operations of claim 1 be "executed in a single clock cycle of the digital signal processor." The operations executing in response to a single instruction and within a single clock cycle of the digital signal processor are both required by claim 1.

Acting in response to a single instruction is not contemplated by Dent. Nowhere in Dent is there any discussion of instructions. Furthermore, executing operations within a single clock cycle is also not contemplated by Dent. Nowhere in Dent is there any discussion relating to clock cycles or the timing of certain operations.

Claim 1 requires the complex multiplication, complex addition and storing all be performed in response to a single instruction. Claim 1 further requires that the complex multiplication, the complex addition and the storing of the despread result are executed in a single clock cycle of the digital signal processor. Dent does not disclose or suggest either of these limitations. Claim 1 is therefore patentable over Dent for at least this reason.

The remaining independent claims, 8, 16, 22, 27 and 28, also contain similar limitations regarding the execution of operations in response to a single instruction and within a single clock cycle. Those claims are therefore patentable for at least the same reasons described above in reference to claim 1. The dependent claims are therefore patentable for at least the same reasons.

Accordingly, withdrawal of the rejection is respectfully requested.

The Özlütürk Reference

In the previous Amendment Applicant argued that claims 1-14 and 16-30 were patentable over Özlütürk because each claim required that the operations of the claims happen "in response to a single instruction," and that the operations of the claims be "executed in a single clock cycle of the digital signal processor." On Page 2 of the most recent Office Action the Examiner indicated that these remarks were persuasive with regards to claims 1-14 and 16-26 but not with regard to claims 27-30. Applicant respectfully requests that the Examiner reconsider the rejection of claims 27-30 in view of Özlütürk.

Claims 27-30 each require that certain operations be executed "in response to a single instruction executed within a single clock cycle of the digital signal processor." Claims 27 and 28 are reproduced below with this phrase underlined:

27. A method for processing a signal value in a digital signal processor, comprising the step of:

in response to a single instruction executed within a single clock cycle of the digital signal processor, specifying a complex signal value and a two bit complex code segment, performing a complex multiply of the signal value by the code segment to provide a processed data value.

(emphasis added).

28. A method for processing signal values in a digital signal processor comprising the steps of:

(a) in response to a single instruction executed within a single clock cycle of the digital signal processor, specifying a set of complex signal values and a corresponding set of complex code segments, performing a complex multiply of each signal value by a corresponding code segment to provide a set of intermediate values; and

(b) in further response to said single instruction performing complex addition of the intermediate values to provide a processed signal value.

(emphasis added).

Both of these claims require the operations to be executed in response to a single instruction and each of these claims require that the operations be executed within a single clock cycle of the digital signal processor. As Applicant has stated in the previous Amendment, Özlütürk does not teach or disclose these limitations.

Özlütürk is directed to a process for improved performance of a data signal decoder. (Abstract). Özlütürk teaches employing a phase-locked loop to eliminate errors due to carrier-offset. (Abstract). Özlütürk teaches signal despreading using a rake receiver and multiple Viterbi decoders (see Fig. 4).

Özlütürk does not disclose or suggest executing the actions of claims 27 or 28 in response to a single instruction. The Office Action does not cite a particular section of Özlütürk to suggest that specific operations occur in response to a single instruction. The Office Action notes, on pages 4-5 that Özlütürk performs operations on a signal value but that signal value is not a single instruction which is executed within a single clock cycle (or within any number of clock cycles) by a digital signal processor. Both claims 27 and 28 require that the single instruction be "executed." In order to be executed, the instruction must be executable. The signal value received by Özlütürk and cited in the Office Action is information data not an executable instruction. Although a digital signal processor may perform operations or processing on the cited signal value (such as complex multiplication or addition) a digital signal processor may not execute the cited signal value as an instruction, which is required by claims 27 and 28.

Furthermore, Özlütürk does not disclose or suggest executing the complex multiplication or complex addition within a single clock cycle of the digital signal processor.

Indeed, the structure of Özlütürk is such that performing those actions within a single clock cycle is not possible. Referring to Özlütürk Fig. 5, for each rake element the pn code sequence is delayed by one chip and mixed with the baseband spread spectrum signal to achieve despreading. (Col. 4, lines 61-64). Özlütürk then states that:

> Each multiplication product is input in an accumulator 109_0, 109_1, 109_2, 109_n, where it is added to the previous product and latched out after the next symbol-clock cycle.

(Col. 4, lines 64-67). As shown in Fig. 5, these accumulators are structured to continue taking input from the complex mixer 107 and to add the results of the mixing in successive clock cycles. The accumulators of Özlütürk are not structured to execute these actions within a single clock cycle. Single clock cycle operation is not contemplated by Özlütürk, or possible given the accumulator structure taught. Özlütürk specifically teaches that inputting a product into an accumulator and adding it to a previous product takes at least two clock cycles. Özlütürk requires a plurality of clock cycles to process the plurality of signal values recited by claims 27 and 28. Claims 27 and 28 requires that the process be executed in a single clock cycle. Özlütürk therefore specifically teaches away from this limitation of claims 27 and 28.

Claim 27 requires that complex multiplication be performed in response to a single instruction. Claim 28 requires that complex multiplication and complex addition be performed in response to a single instruction. Claims 27 and 28 both further require that the complex operations be executed in a single clock cycle of the digital signal processor. Özlütürk does not disclose or suggest either of these limitations. Claims 27 and 28 are therefore patentable over Özlütürk for at least this reason. Claims 29 and 30 depend from claim 28 and therefore incorporate the limitations of claim 28 and are patentable for at least the same reason.

This argument was presented to the Examiner with regard to claims 1-14 and 16-26 and was found to be persuasive. Because the limitations upon which this argument was based (the single instruction and single clock cycle) appear in claims 27-30 Applicant respectfully request that the Examiner reconsider the rejection of claims 27-30 under Özlütürk.

Accordingly, withdrawal of the rejection is respectfully requested.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
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